EXPRESS MAIL LABEL NO.:

(EL708269968US)

INTELLIGENT DELAY INSERTION BASED ON TRANSITION

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BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to a method and system using delay signals to reduce or eliminate interference between paths in a communication network, in particular an electronic circuit.

DESCRIPTION OF THE RELATED ART

Communication networks, in particular communication networks on integrated circuits, have numerous paths carrying signals from one device to other devices. Multiple paths that are placed near one another can lead to problems related to coupling and capacitative interference. The situation becomes most problematic when multiple paths carrying signals that transition or switch at the same time, run parallel to a single path switching in the opposite direction.

Coupling effects do not have a noticeable effect upon signals that are switching in the same direction. In a digital signal transmission, the rise of the signal from a driver connected to a path is not affected by signals from the other paths switching in the same direction. Coupling effects, however, can have an effect upon the paths whose signals switch in the opposite direction. In particular coupling effects lead to slower rise times of path signals. To compensate for slower rise times, path driver power is increased. Path drivers are required to provide additional power to compensate for a slower rise time in order to get signals out and to achieve proper signal level and timing requirements.

In certain designs, neutral paths such as ground paths, also known as shield lines, are available and placed between aggressors and victim paths, effectively shielding the opposite switching paths from one another. Shield lines typically serve no function but are merely used to shield the victim path. The use of neutral paths or shield lines also leads to design considerations and network architecture constraints in laying out paths. Adding shield lines further adds to an increase in the space of the network. In an integrated circuit, minimizing size is highly desirable, and adding non-functional shield lines becomes counter productive to meeting the goal of minimizing size.

SUMMARY OF THE INVENTION

In one embodiment, a method of transmitting a signal is disclosed. The method includes sensing adjacent signals and delaying certain adjacent signals until switching or transition takes place with the other adjacent signal or signals.

In certain embodiments, various number signal groups including two-signal, three-signal, and five-signal groups sense and delay for particular signals. Signals that are adjacent to more than one signal are delayed in the event that any or all of the adjacent signals simultaneously switch with the particular signals.

In certain embodiments, a separate sensing and delay circuit is provided. Along with buffers, the sensing and delay circuit provides a delay signal to the buffers in the event that adjacent signals switch simultaneously, thus delaying an adjacent signal.

In other embodiments, the method assigns priorities to transmitted signals. Signals that have a lower priority compared to signals with a higher priority are delayed until the higher priority signals are switched. In certain embodiments, a delay pulse is sent to by the higher priority signal or signals to the lower priority signal or signals.

The foregoing is a summary and thus contains, by necessity, simplifications, generalizations and omissions of detail; consequently, those skilled in the art will appreciate that the summary is illustrative only and is not intended to be in any way limiting. Other aspects, inventive features, and advantages of the present invention, as defined solely by the claims, will become apparent in the non-limiting detailed description set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the figures designates a like or similar element.

Fig. 1A is a diagram illustrating the use of inverter delays to avoid coupling interference.

Fig. 1B is a timing diagram illustrating a three-signal group with delay provisioning.

Fig. 1C is a timing diagram illustrating a five-signal group with delay provisioning.

Fig. 1D is a timing diagram illustrating a five-signal group with delay provisioning when three adjacent signals switch simultaneously.

Fig. 1E is a timing diagram illustrating a five-signal group with an extended delay when initial delay results in simultaneously switching with an adjacent signal.

Fig. 2 is a block diagram illustrating use of a sensing and delay circuit and buffers to transition a three-signal group.

Fig. 3 is a flow diagram illustrating transition of adjacent signals for a three-signal group.

Fig. 4 is a block diagram illustrating use of a sensing and delay circuit and buffers to transition a five-signal group.

Fig. 5 is a flow diagram illustrating transition of adjacent signals for a five-signal group.

Fig. 6 is a block diagram of three and five signal groups with shield lines.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail, it should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed but

on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION

The following is intended to provide a detailed description of an example of the invention and should not be taken to be limiting of the invention itself. Rather, any number of variations may fall within the scope of the invention which is defined in the claims following the description.

Introduction

The present invention provides a method and apparatus for avoiding or minimizing coupling interference in adjacent paths in a communication network by sensing transitioning (switching) instances of adjacent paths and delaying a signal from transitioning while adjacent signal(s) transitions. Coupling interference is avoided between the adjacent signal paths by assuring sufficient time differences exist between the transitioning of the adjacent signals. A signal transitions (switches) without coupling interference from a simultaneously switching adjacent signal.

Delay Signals

Fig. 1A is a diagram illustrating the use of inverter delays to avoid coupling interference. Signal 1 100 is an adjacent signal to Signal 2 105. Signal 2 105 is an adjacent signal to Signal 3 110. In order to avoid coupling interference, in particular when Signal 1 100, Signal 2 105, and Signal 3 110 are switching, a delay is provided in the form of an inverter 115 along the path of Signal 2 105. Switching of a signal takes place on either a rising or falling edge of the signal. In this particular example, the signals are digital signals representing either a "1" or "0" value. Signal 2 105 is restored later along the transmission line is by inverter 120. In other words, the signal 2 105 is inverted once again to restore the original transmitted value prior to inverter 115. The path of inverted Signal 2 105 is presented by path length 125. Because of the delay from inverter 115 and 120, a non-coupling zone 125 is provided assuming signal 2 105 is not delayed such that signal 2 105 switches at the same time as signal 1 100 and/or signal 3 110. Within non-coupling zone 130, there is a small likelihood of coupling interference between signals 100, 105 and 110,

assuming that delay to Signal 2 105 would not cause Signal 2 105 to couple with Signal 1 100 and Signal 3 110.

Fig. 1B is a timing diagram illustrating a three-signal group with delay provisioning. Signal 1 100, signal 2 105, and signal 3 110 are part of a three-signal group with signal 2 105 placed between signal 1 100 and signal 3 110. Whenever signals 100 and 105, or signals 105 and signal 110 switch simultaneously, in this particular example the three signals 100, 105, 110 are switching at time T1 115, a delay is performed by delay logic 120. Delay logic 120 provides a sufficient delay to signal 2 105 in order to prevent simultaneous switching with signal 1 100 and/or signal 3 110. Signal 2 105 switches at time T2 125. The delay is a d 130. Delay d 130 can be a predetermined period of time or any amount of time sufficient to prevent simultaneous switching with signal 2 105 and adjacent signal 1 100 and signal 3 110. The delay avoids any coupling interference in the event that signal 2 105 is an opposite switching signal to either signal 1 100 and/or signal 3 110.

Fig. 1C is a timing diagram illustrating a five-signal group with delay provisioning. Signal 1 100, signal 2 105, signal 3 110, signal 4 135 and signal 5 140 are adjacent to one another in order. In this particular example, all five signals are switching at the same time, time T1 115. In this particular embodiment, delay logic 120 delays signal 1 100, signal 3 110, and/or signal 5 140 whenever simultaneous switching occurs with adjacent signal 2 105 and/or signal 4 135. Signal 2 105 and signal 4 135 are never delayed, and are allowed to switch at their initial switching time, in this case time T1 115. In this example, signal 1 100, signal 3 110, and signal 5 140 are delayed and switch at time T2 125. The delay d 130 can be a predetermined period or any sufficient amount of time that prevents simultaneous switching of signals. The delay avoids any coupling interference between adjacent simultaneously switching signals.

Fig. 1D is a timing diagram illustrating a five-signal group with delay provisioning when three adjacent signals switch simultaneously. In this particular example, signal 1 100 and signal 5 140 simultaneously switch at time T1 115. Signal 1 100 and signal 5 140 are far enough apart that simultaneously switching does not affect the respective signals. Signal 2 105, signal 3 110, and signal 4 135 simultaneously switch at time T3 145. In order to avoid any coupling interference, specifically if signal 3 110 is an opposite switching signal to signal 2 105 and/or signal 4 135, delay logic 120 delays signal 3 110. Signal 2 105 and signal 4

135, in this embodiment, are never delayed and switch at their respective original switch time T3 145. Signal 3 110 is switched at time T4 150, providing a delay of d 130. Delay d 130 can be a predetermined period of delay of any amount of delay sufficient to avoid simultaneously switching of adjacent signals.

Fig. 1E is a timing diagram illustrating a five-signal group with an extended delay when initial delay results in simultaneously switching with an adjacent signal. In this particular embodiment of the invention, signal 2 105 and signal 4 135 are never delayed, and always switch at their respective original switch times, in this example signal 2 105 switches at time T1 115and signal 4 135 switches at time T3 145. Signal 1 100, signal 3 110, and signal 5 140 switch at time T1 115, the same time that signal 2 105 switches. Delay logic 120 senses that adjacent signal 1 100 and signal 3 110 switch at the same time as signal 2 105, therefore a delay is provided to signal 1 100 and signal 3 110. Signal 1 100 now switches at time T3 145, the same time as signal 4 135, however the two signals are far enough removed from one another to avoid any coupling interference. Signal 3 110 would also be delayed to time T3 145, however, this condition would result in signal 3 110 switching at the same time as signal 4 135. Delay logic 120 therefore provides for signal 3 110 to be further delayed to time T5 155. The adjusted delayed timing diagram prevents adjacent signals from switching at the same times and avoids coupling interference when adjacent signals are switching opposite one another.

Sensing and Delay Logic

Fig. 2 is a block diagram illustrating use of a sensing and delay circuit and tri-state buffers to transition signals. Signals 100, 105, and 110 are monitored by sensing and delay circuit 200. Sensing and delay circuit 200 receives sense signals 205, 210, and 215 respectively from signal 1 100, signal 2 105, and signal 3 110. Sensing and delay circuit 200 determines if signal 2 105 switches at the same time as signal 1 100 and/or signal 3 110. If signal 2 105 switches at the same time as either adjacent signal 1 100 or adjacent signal 3 110, signal 2 105 is delayed. In this example, buffers 220 and 230 are buffers to match the delay of tri-state buffer 225 when there is no simultaneous switching. Tri-state buffer 225 provides for three possible values: a value of 0, 1, or a high impedance value. A signal may be switching on the rising edge, therefore a value of 1 is associated with it. A signal that is switching on the falling edge has a value of 0. A signal that has been delayed or is awaiting

transition from sensing and delay circuit 200 maintains its binary signal value. The use of sensing and delay circuit 200 along with buffers 220, 225, and 230 assure that signal 1 100 and 3 110 are always immediately passed through. Signal 2 105 is immediately passed through without delay unless signal 2 105 switches at the same time as Signal 1 100 or Signal 3 110. Since signal 1 100 is far enough removed from signal 3 110, possibility of coupling interference between signal 1 100 and signal 3 110 is minimal.

Fig. 3 is a flow diagram illustrating transition of adjacent signals for a three signal group. Sensing and delay circuit 200 receives signals 100, 105, and 110, step 300. Signals 100 and 105 are sensed at the same time, step 305. Simultaneously signals 105 and 110 are also sensed with one another at the same time, step 310. A determination is made if signals 100 and 105 are switching at the same time, step 315. A determination is also made whether signals 105 and 110 are switching at the same time, step 320. If the condition is true for either steps 315 or 320, then signal 2 105 is delayed, step 325. If steps 315 and 320 are both determined to be "no," then signal 2 105 is not delayed, step 330.

Fig. 4 is a block diagram illustrating use of a sensing and delay circuit and buffers to transition a five-signal group. Buffer 400 is used for signal 1 100. Buffer 405 is used for signal 2 105. Buffer 410 is used for signal 3 110. Buffer 415 is used for signal 4 135. Buffer 420 is used for signal 5 140. Buffers 400, 410, and 420 are tri-state buffers that receive delay signals from sensing and delay circuit 425. A received delay signal to the respective buffer tri-states the respective signals. In this particular example delay signal 430 is provided to buffer 420. Delay signal 435 is provided to buffer 410. Delay signal 440 is provided to buffer 400. Sensing and delay circuit 425, in this embodiment, includes three separate circuit or logic blocks: sensing and delay circuit A 445; sensing and delay circuit B 450; and sensing and delay circuit A 455. The respective sensing and delay circuits can include digital, analog, and/or combined circuits that sense and hold signals and trigger respective tri-state buffers 400, 405, 410, 415, and 420. In this particular embodiment, sensing and delay circuit A 445 senses signal 1 100 through sense signal 460 and signal 2 105 through sense signal 465. Sensing and delay circuit B 450 senses signal 2 105 through sense signal 470, signal 3 110 through sense signal 475, and signal 4 135 through sense signal 480. Sensing and delay circuit A 455 senses signal 4 135 through sense signal 485 and signal 5 140 through sense signal 490. The use of sensing and delay circuit 425, in particular sensing and delay circuit 450 and tri-state buffer 410 to delay signal 3, provides a uninterrupted continuous delay.

Delay signal 435 is provided to tri-state buffer 410 whenever the delay actually is required to take place. This prevents separate delay glitches that can cause aberrations in signal transmission.

Fig. 5 is a flow diagram illustrating transition of adjacent signals for a five-signal group. Fig. 5 specifically illustrates the logic involved in the block diagram and the sensing and delay circuits of Fig. 4. As in a three-signal group, contention is provided for a five-signal group using a sensing and delay circuit or similar logic. Other multiple signal groups can also make use of such logic and similar sensing and delay circuit (logic). In this example, the sensing and delay circuit receives five signals, signals 1, 2, 3, 4 and 5, step 500. Signals 1, 2, 3, 4, and 5 in order are adjacent to one another in the group. In other words, signal 1 is adjacent to signal 2; signal 2 is adjacent to signal 3; signal 3 is adjacent to signal 4; and signal 4 is adjacent to signal 5. Signals 1 and 2 are sensed with one another, step 505. Signals 2 and 3 are sensed with one another, step 510. Signals 3 and 4 are sensed with one another, step 515. Signals 4 and 5 are sensed with one another, step 520. A determination is made as to whether Signals 1 and 2 are transitioning (switching) at the same time, step 525. If step 525 is determined to be "yes" then Signal 1 is delayed, step 530. If step 525 is determined to be "no" then Signal 1 is not delayed, step 535. A determination is made as to whether adjacent signals 4 and 5 are transitioning at the same time, step 540. If step 540 is determined to be "yes" then signal 5 is delayed, step 545. Since signal 3 is the middle signal of the five-signal group and is directly adjacent to signals 2 and 4, signal 3 is delayed if signal 3 transitions at the same time as either signal 2 or signal 4. A separate determination is made as to whether signals2 and 3 are transitioning at the same time, step 555. Another determination is made as to whether signals 3 and 4 are transitioning at the same time, step 560. If either step 555 or step 560 is "yes," signal 3 is delayed, step 565. If both step 555 and step 560 are "no" then Signal 3 is not delayed, step 570.

Fig. 6 is a block diagram of three and five signal groups with shield lines. Sensing and delay circuits can be placed before, after, or in signal drivers. The signal drivers transmitting the signal after delay is provided to the signal. In order to maximize the use of sensing and delay circuits, signals are grouped together and use a single sensing and delay circuit. Signal group 600 is a group of three signals. Signal group 605 is another group of three signals. Groups 600 and 605 can be placed near one another; however, to prevent any coupling between the adjacent signals of the two groups, a shield line 610 is added. Signals

in groups 600 and 605 can be placed relatively near one another through the use of the sensing and delay circuits, however some protection and spacing is provided by way of shield line 610. In a similar manner groups of five-signal groups can be provided as illustrated by signal groups 615 and 620, and separated by shield line 625. Other multiple number signal groups can be provided, and variations are possible in the use of various groupings of signals and shield lines. Groupings and use of shield lines are dependent on the circuit or network architecture that is desired.

Although the present invention has been described in connection with several embodiments, the invention is not intended to be limited to the specific forms set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as can be reasonably included with in the scope of the invention as defined by the appended claims.